applicant respectfully traverses this rejection, and presents below [in brackets] exemplary references to the body of the application which support the recited limitations of claims 3-6.

Regarding amended claim 3 – "An integrated circuit according to claim 2, wherein said first bipolar transistor [Q33:c.f. p. 5, lines 15-18] is a vertical transistor having an emitter formed by said substrate [c.f. p. 5, line 16; p. 6, lines 28-29], a collector formed by a second doped region [c.f. p. 5, lines 15-16; p. 6, lines 29-30; Figure 7, region 36] of the first conductivity type [N type: c.f. p. 6, line 29; Figure 7, region 36], and a base formed by a first doped region [c.f. p. 5, lines 17-18; p. 6, lines 27-28; Figure 7, region 37] of the second conductivity type [P type: c.f. p. 6, line 27; Figure 7, region 37] formed in the substrate, and within the first doped region. [c.f., p.6, lines 20-30]"

Regarding amended claim 4 – "An integrated circuit according to claim 3, wherein said first [Q33:c.f. p. 5, lines 15-18] and third [Q11:c.f., p. 6, lines 23-26] bipolar transistors are isolated from the substrate by said isolation region [c.f., p.6, lines 23-25 and 26-28]."

Regarding Claim 5 – "An integrated circuit according to claim 4, wherein said first conductivity type is N type, said second conductivity type is the P type [c.f. p. 6, lines 20-33; Figure 7], said first [Q33] and second [Q22] bipolar transistors are NPN transistors, [c.f. p. 5, line 15; p. 5, line 22, respectively], and said third bipolar transistor [Q11] is a PNP transistor [c.f. p. 5, line 19]."

Regarding Claim 6 – "An integrated circuit according to claim 1, wherein said vertical power component is a vertical power bipolar transistor [c.f. p. 1, lines 14-21; p. 5, lines 31-32]."

Having thus provided specific support in the application for the claims in question, the applicant respectfully requests that the rejection under 35 U.S.C. §112, first paragraph, now be withdrawn and the claims be allowed.

Claim Rejections under 35 U.S.C. §103

The Office Action rejected claims 1-6, at paragraph 5 of the Office Action, as being unpatentable over Aiello et al. (5,382,837) under U.S.C. §103(a), stating that "*Aiello et al.'s structure is identical to the claimed structure.*" Office Action, p. 4, middle. The applicant respectfully traverses this rejection for at least the following reasons. First, the Office Action has mischaracterized Aiello. Second, no motivation is presented that would lead one of ordinary

skill in the art to make the modifications to Aiello which are suggested in the Office Action. The applicant requests that these rejections be withdrawn and the claims be allowed.

Aiello discloses a switching circuit that connects a first circuit node to either a second or a third circuit node relative to a voltage potential on the third circuit node, as shown in Aiello's Figure 1. Two of the three transistors in Aiello share a common collector and are connected in series. Aiello shows two embodiments thereof in Figures 6 and 10, referred to in the Office Action.

The Office Action's characterization of Aiello is improper

The Office Action refers to Figures 6 and 10 of Aiello, at paragraph 5 of the Office Action, and states that "*although Aiello et al. do not teach using the device as a protection structure against polarity inversion... this feature is inherent in Aiello et al.'s device, because Aiello et al.'s structure is identical to the claimed structure*." The applicant respectfully disagrees with the characterization of the circuit of Aiello in the Office Action, and believes that the parenthetical qualifications provided in the Office Action are improper. The applicant also disagrees with the conclusions made in the Office Action regarding the use of the claimed device. The applicant presents below arguments showing that the structure of Aiello is not identical to the claimed structure and that the features of the claimed structure are not thus inherent in Aiello.

Contrary to what is stated in the Office Action at paragraph 5, the first transistor T2 of Aiello does not have an emitter connected to the isolation region. The emitter of transistor T2 in Aiello is rather connected to the collector 53 instead of being connected to the isolation region 5, 34 as asserted in the Office Action. The Office Action, states that "*transistor T2 [has] an emitter connected to the isolation region (via base and collector regions)*." This does not support the notion that Aiello's transistor T2 has an emitter connected to the isolation region as claimed by the applicant.

Furthermore, the collector of transistor T2 is connected to region 36 of Aiello and not to a reference potential input. At paragraph 5 of the Office Action, the Office Action asserts "*a collector connected to a reference potential input of the integrated circuit (via transistor T1)*,"

this is a mischaracterization of Aiello and does not support that transistor T2 has a collector connected to a reference potential input.

Accordingly, the applicant thus respectfully disagrees with the Office Action's characterization Aiello, and believes that the parenthetical qualifications provided in the Office Action to show the interconnection of various elements in the circuit are improper.

No motivation to modify Aiello as implied by the Office Action

Contrary to the assertions of the Office Action stating that "*Aiello et al.'s structure is identical to the claimed structure*," (Office Action, p. 4, middle), the Office Action itself points to modifications (discussed above) to Aiello that would presumably make the applicant's claims read on Aiello's circuits. Even if these modifications, would yield the result as per the Office Action, no motivation exists for one of ordinary skill in the art to make such modifications.

More specifically, paragraph 5 of the Office Action, states that "*transistor T2 [has] an emitter connected to the isolation region (via base and collector regions)*." The statement suggests that one of ordinary skill in the art would desire to modify the circuit of Aiello to connect the emitter of T2 to the isolation region, as the emitter of T2 is not connected to the isolation region in Aiello. Likewise, at the same paragraph, the Office Action asserts "*a collector connected to a reference potential input of the integrated circuit (via transistor T1)*," again, suggesting that one of ordinary skill in the art would modify the circuit of Aiello to connect transistor T2's collector to a reference potential input, since Aiello does not explicitly disclose such a connection. Neither of these modifications is motivated in the record, hence, a prima facie case for the obviousness rejection of the applicant's claims in view of Aiello has not been made.

In contrast to Aiello, claim 1 recites an integrated circuit including, inter alia, "A first bipolar transistor with an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit." As discussed above, Aiello does not teach or suggest at least this limitation. Accordingly claim 1 distinguishes over Aiello and is in allowable condition. Withdrawal of the rejection of the claim under 35 U.S.C. §103(a) is respectfully requested.

Claims 2-6 depend from claim 1 and are allowable for at least the same reasons.

Newly-presented claim 7 recites, inter alia, "*a protection structure against polarity inversion of a substrate potential, comprising...a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit.*" As discussed above, at least these limitations are not disclosed or suggested in the art of record, and therefore claim 7 patentably distinguishes over such art.

Claims 8-9 depend from claim 7 and are allowable for at least the same reasons.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,

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Attorney's Docket No. S1022/8385
Dated: February , 2002
2/28/02

AMENDED TITLE

Please replace the current title

AN INTEGRATED CIRCUIT INCLUDING A VERTICAL POWER COMPONENT, A CONTROL CIRCUITRY THEREOF, AND A PROTECTION STRUCTURE AGAINST POLARITY INVERSION OF THE SUBSTRATE POTENTIAL

with

-- AN INTEGRATED CIRCUIT INCLUDING PROTECTION AGAINST POLARITY INVERSION OF THE SUBSTRATE POTENTIAL--.

Claim Version with Markings to Show Changes Made

3. (Amended) An integrated circuit according to claim 2, wherein said first bipolar transistor is a vertical transistor having an emitter formed by said substrate, [a base formed by a first doped region of the second conductivity type formed in the substrate, and] a collector formed by a second doped region of the first conductivity type [formed within the first doped region], and **a base formed by a first doped region of the second conductivity type formed in the substrate and formed within the first doped region**.

4. (Amended) An integrated circuit according to claim 3, wherein said [second] **first** and third bipolar transistors are isolated from the substrate by said isolation region.